IN THE CLAIMS:

1.-11 (Cancelled)

12. (Currently Amended) A voltage controlled oscillator ~~according to claim 11, further~~ circuit, comprising:

a first node connected to a first power source having a first voltage;

a second node connected to a second power source having a second voltage;

a first MOS transistor;

an oscillator arranged between the first node and a third node; and

a first capacitive element arranged between the first node and the third node;

a second capacitive element; and

a node to the second capacitive element;

wherein an oscillation frequency of the oscillator is controlled by connecting a source of the first MOS transistor to the second node, connecting a drain of the first MOS transistor to the third node, applying an analog control signal to a gate of the first MOS transistor, and changing a frequency of a high level and a low level of a digital control signal; and

connection to and disconnection from the second capacitive element are selected according to the digital control signal.

13. (Currently Amended) A voltage controlled oscillator circuit according to claim 12, wherein the oscillator includes at least three inverters each formed by

connecting a drain of a P-channel MOS transistor to a drain of an N-channel MOS transistor; and

wherein the inverters are looped by sequentially connecting respective output terminals of the inverters to respective input terminals of the inverters.

14. (Currently Amended) A phase-locked loop (PLL) circuit, comprising:

a voltage controlled oscillator circuit according to claim 13;

a frequency divider;

a phase comparator;

a frequency comparator; and

a control circuit;

wherein the frequency divider outputs a divided output signal obtained by dividing a frequency of an output signal from the voltage controlled oscillator circuit;

wherein the phase comparator receives a reference signal and the divided output signal, compares a phase of the reference signal with a phase of the divided output signal, and outputs a phase difference detection signal;

wherein the frequency comparator receives the reference signal and the divided output signal, compares a frequency of the reference signal with a frequency of the divided output signal, and outputs a frequency difference detection signal;

wherein the control circuit receives the phase difference detection signal and the frequency difference detection signal and outputs the analog control signal to execute control according to the phase difference detection signal and the frequency difference detection signal; and

wherein the phase difference detection signal corresponds to the digital control signal.

15. (Previously Presented) A phase-locked loop (PLL) circuit according to claim 14, wherein the control circuit also receives the reference signal;

wherein the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle of the reference signal; and

wherein a variation of a voltage of the analog control signal according to the frequency difference detection signal is larger than a variation of the voltage of the analog control signal according to the phase difference detection signal.

16. (Previously Presented) A phase-locked loop (PLL) circuit according to claim 14, wherein the control circuit has a control cycle in which the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle of the reference signal; and

wherein the frequency comparator includes

means for comparing the frequency of the reference signal with the frequency of the divided output signal, and

means for preventing a variation of a voltage of the analog control signal according to the phase difference detection signal in a first control cycle in which the frequency difference detection signal corresponding to a detection of a

frequency difference is outputted and in a predetermined number of control cycles following the first control cycle.

17. (Currently Amended) A phase-locked loop (PLL) circuit, comprising:

a voltage controlled oscillator circuit according to claim 12;

a frequency divider;

a phase comparator;

a frequency comparator; and

a control circuit;

wherein the frequency divider outputs a divided output signal obtained by dividing a frequency of an output signal from the voltage controlled oscillator circuit;

wherein the phase comparator receives a reference signal and the divided output signal, compares a phase of the reference signal with a phase of the divided output signal, and outputs a phase difference detection signal;

wherein the frequency comparator receives the reference signal and the divided output signal, compares a frequency of the reference signal with a frequency of the divided output signal, and outputs a frequency difference detection signal;

wherein the control circuit receives the phase difference detection signal and the frequency difference detection signal and outputs the analog control signal to execute control according to the phase difference detection signal and the frequency difference detection signal; and

wherein the phase difference detection signal corresponds to the digital control signal.

18. (Previously Presented) A phase-locked loop (PLL) circuit according to claim 17, wherein the control circuit also receives the reference signal;

wherein the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle corresponding to one cycle of the reference signal; and

wherein a variation of a voltage of the analog control signal according to the frequency difference detection signal is larger than a variation of the voltage of the analog control signal according to the phase difference detection signal.

19. (Previously Presented) A phase-locked loop (PLL) circuit according to claim 17, wherein the control circuit has a control cycle in which the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle of the reference signal; and

wherein the frequency comparator includes

means for comparing the frequency of the reference signal with the frequency of the divided output signal, and

means for preventing a variation of a voltage of the analog control signal according to the phase difference detection signal in a first control cycle in which the frequency difference detection signal corresponding to a detection of a frequency difference is outputted and in a predetermined number of control cycles following the first control cycle.

20. (Currently Amended) A voltage controlled oscillator ~~according to claim 11, further~~ circuit, comprising:

a first node connected to a first power source having a first voltage;

a second node connected to a second power source having a second voltage;

a first MOS transistor;

an oscillator arranged between the first node and a third node; and

a first capacitive element arranged between the first node and the third node;

a ~~third~~ second capacitive element; and

a second MOS transistor;

wherein an oscillation frequency of the oscillator is controlled by connecting a source of the first MOS transistor to the second node, connecting a drain of the first MOS transistor to the third node, applying an analog control signal to a gate of the first MOS transistor, and changing a frequency of a high level and a low level of a digital control signal;

~~wherein~~ the second MOS transistor is used for a switch to the ~~third~~ second capacitive element; and

~~wherein~~ connection to and disconnection from the ~~third~~ second capacitive element are selected by inputting the digital control signal to a gate of the second MOS transistor.

21. (Previously Presented) A voltage controlled oscillator according to claim 20, wherein the oscillator includes at least three inverters each formed by connecting

a drain of a P-channel MOS transistor to a drain of an N-channel MOS transistor; and

wherein the inverters are looped by sequentially connecting respective output terminals of the inverters to respective input terminals of the inverters.

22. (Currently Amended) A phase-locked loop (PLL) circuit, comprising:

a voltage controlled oscillator circuit according to claim 21;

a frequency divider;

a phase comparator;

a frequency comparator; and

a control circuit;

wherein the frequency divider outputs a divided output signal obtained by dividing a frequency of an output signal from the voltage controlled oscillator circuit;

wherein the phase comparator receives a reference signal and the divided output signal, compares a phase of the reference signal with a phase of the divided output signal, and outputs a phase difference detection signal;

wherein the frequency comparator receives the reference signal and the divided output signal, compares a frequency of the reference signal with a frequency of the divided output signal, and outputs a frequency difference detection signal;

wherein the control circuit receives the phase difference detection signal and the frequency difference detection signal and outputs the analog control signal to execute control according to the phase difference detection signal and the frequency difference detection signal; and

wherein the phase difference detection signal corresponds to the digital control signal.

23. (Previously Presented) A phase-locked loop (PLL) circuit according to claim 22, wherein the control circuit also receives the reference signal;

wherein the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle of the reference signal; and

wherein a variation of a voltage of the analog control signal according to the frequency difference detection signal is larger than a variation of the voltage of the analog control signal according to the phase difference detection signal.

24. (Previously Presented) A phase-locked loop (PLL) circuit according to claim 22, wherein the control circuit has a control cycle in which the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle of the reference signal; and

wherein the frequency comparator includes

means for comparing the frequency of the reference signal with frequency of the divided output signal, and

means for preventing a variation of a voltage of the analog control signal according to the phase difference detection signal in a first control cycle in which the frequency difference detection signal corresponding to a detection of a

frequency difference is outputted and in a predetermined number of control cycles following the first control cycle.

25. (Currently Amended) A phase-locked loop (PLL) circuit, comprising:

a voltage controlled oscillator circuit according to claim 20;

a frequency divider;

a phase comparator;

a frequency comparator; and

a control circuit;

wherein the frequency divider outputs a divided output signal obtained by dividing a frequency of an output signal from the voltage controlled oscillator circuit;

wherein the phase comparator receives a reference signal and the divided output signal, compares a phase of the reference signal with a phase of the divided output signal, and outputs a phase difference detection signal;

wherein the frequency comparator receives the reference signal and the divided output signal, compares a frequency of the reference signal with a frequency of the divided output signal, and outputs a frequency difference detection signal;

wherein the control circuit receives the phase difference detection signal and the frequency difference detection signal and outputs the analog control signal to execute control according to the phase difference detection signal and the frequency difference detection signal; and

wherein the phase difference detection signal corresponds to the digital control signal.

26. (Previously Presented) A phase-locked loop (PLL) circuit according to claim 25, wherein the control circuit also receives the reference signal;

wherein the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle corresponding to one cycle of the reference signal; and

wherein a variation of a voltage of the analog control signal according to the frequency difference detection signal is larger than a variation of the voltage of the analog control signal according to the phase difference detection signal.

27. (Previously Presented) A phase-locked loop (PLL) circuit according to claim 25, wherein the control circuit has a control cycle in which the control circuit executes control according to the phase difference detection signal and the frequency difference detection signal every cycle of the reference signal; and

wherein the frequency comparator includes

means for comparing the frequency of the reference signal with the frequency of the divided output signal, and

means for preventing a variation of a voltage of the analog control signal according to the phase difference detection signal in a first control cycle in which the frequency difference detection signal corresponding to a detection of a frequency difference is outputted and in a predetermined number of control cycles following the first control cycle.

28.-34. (Cancelled)